Institut für Parallele und Verteilte Systeme – Parallele Systeme

Master Thesis

Design and Implementation of a Reliable Data Transmission System Based on 10 Gigabit Ethernet

In many applications such as high-performance data acquisition, a high bandwidth and reliable data transfer is required. The 10 Gigabit Ethernet offers a fast interconnectivity for such applications. The goal of this thesis is to develop a high performance and reliable data transmission system based on 10 Gigabit Ethernet using Xilinx Kintex-7 FPGAs. Xilinx Kintex-7 FPGAs integrate multiple high performance transceivers. Using these transceivers, the PCS/PMA sublayers and MAC sublayer are implemented for 10 Gigabit Ethernet with soft core provided by Xilinx. In this thesis, a reliable transmission system based on User Datagram Protocol (UDP) needs to be designed and implemented on FPGA. The parallel architecture should be studied, and the proposed design should be optimized with respect to operating frequency and resource utilization. In addition, a packet loss recovery method should be developed.

The thesis includes the following tasks:

- Study parallel architectures for the FPGA implementation of the UDP/IP stack.
- Design and implementation of a UDP/IP protocol over the 10-gigabit Ethernet.
- Development of a packet loss recovery method based on UDP.
- Validation and testing of the implementation.

Prerequisites:

- Advanced knowledge of VHDL (1 years+)
- Good knowledge of network protocols
- Experience with Xilinx Tools, Modelsim
- Ability to work independently

Preferred:

- Experience with Xilinx Vivado

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